REMARKS

These amendments are made to put the application in compliance with the amendments filed in the parent application, Serial Number 09/573,042 on June 1, 2000.

ARGUMENT

In the office action mailed on October 1, 2001 for the parent application, Claims 1 through 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 5,288,949 to Crafts (hereinafter "Crafts") in view of the article Minimum Crosstalk Channel Routing by Tong Gao and C.L. Liu (hereinafter "Gao").

Crafts teaches arranging the conductors in a Multi-chip Module ("MCM") such that both power supply conductors and ground conductors are interwoven around signal conductors, and provide shielding for the signal conductors, thus reducing cross-talk. (Crafts at Abstract). Crafts teaches that two of the important features of the invention are the following:

> "2. Each signal trace, along nearly its entire length, is flanked by a pair of power supply grids. This flanking shield the signal trace and reduces cross-talk among the signal traces." (Crafts at column 3, lines 10-15).
>
> "9. There may be regions in which the signal traces will not be flanked by the power grids; that is, in these regions, the signal traces can exist outside the unit cells of FIG. 10. ... However, it is expected that these two regions will account for less than 5 to 10 percent of the length of the signal traces, and thus the signal traces can be viewed as substantially contained within the

> period array of unit cells." (Crafts at column 5, lines 38-49).

Therefore, it is clear that Crafts teaches a system of arranging signal conductors such that each signal conductor is flanked by a power supply grid, thus shielding each signal trace. Further, since at most only 5-10 percent of the length of the signal traces will not be flanked by the supply grid, the signal traces can and will still be viewed as being shielded. Hence, any sort of optimization with respect to reducing cross-talk in Crafts would change Craft's principle of placing each and every signal trace adjacent to two power supply grids.

The examiner states the following:

> "Crafts...does not teach optimizing the routing based on a crosstalk minimization criterion to take maximum advantage of their disclosed electromagnetic principle. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the routing as disclosed by Crafts in order to minimize the crosstalk, and it would have further been obvious to one of ordinary skill in the art at the time of the invention to incorporate such a minimization criterion during routing into the teachings of Crafts..." Office action at page 6, paragraph 16.

The examiner further states:

> "Crafts further does not disclose ranking of: 1) the criticality of the line and 2) the preferred tracks. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate these two features into the teachings of Craft for the following reasons. At least two issues are present (inherent)

> during consideration of routing: 1) what wire to rout and 2) where to rout the chosen wire. Clearly these choices must be made before routing." Office action at pages 6-7, paragraph 16.

The examiner's proposal of ranking the criticality of the lines and ranking the preferred tracks of Crafts would change the simple principle of Crafts, which is to flank each signal line with a power supply grid. The MPEP states as follows:

> "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the reference are not sufficient to render the claims *prima facie* obvious. *In re Ratti,* 270. F.2d 810, 123 USPQ 349 (CCPA 1959)" MPEP 2143.01 at page 2100-125.

Further, one of the advantages of Crafts is that it provides "an economic advantage over the prior art approaches." Crafts states the following:

> "In this prior-art spacing, only one-fourth of the surface area of the MCM is covered by the signal traces; the rest (i.e., the 75 μM spacings) is blank. The invention eliminates this wasted space by positioning the power supply grids in the space, and eliminating the plates." Crafts at column 4, lines 11-16.

If Crafts were to be combined with Gao, then necessarily many of the signal traces would no longer be flanked by the power supply grid, thus requiring optimization of routing parameters. Since the signal traces would no longer be flanked and therefore shielded by the power supply grid, the signal traces would therefore

would require the 75 μM spacings between signal traces (see Crafts at column 4, lines 6-10), which would make Crafts unsatisfactory for a purpose of saving this wasted space.

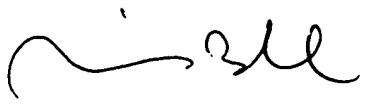
The MPEP states:

> "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon,* 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143 at page 2100-124.

The examiner's proposed modification to Crafts would render Crafts unsatisfactory for its intended purpose of providing a simple shielding scheme for the signal traces. Thus, there can be no suggestion or motivation to combine Crafts with Gao.

Based upon the above, it is respectfully submitted that the examiner has failed to make a *prima facie* case for obviousness, and his rejections should be withdrawn.

Respectfully submitted,



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Michael A. Blake
Reg. No. 42,333

Sierra Patent Group
P.O. Box 6149
295 Highway 50, Suite 20
Stateline, Nevada 89449

Telephone: (775) 586-9500
Facsimile: (775) 586-9550

MARKED UP SPECIFICATION

In the specification kindly amend as follows:

Replace the paragraph on page 5, lines 13-17 with the following paragraph:

For example, in FIG. 4, critical [sensitive] conductor 52 has been placed by the analyzer in the location depicted, immediately adjacent to noisy conductor 54. A critical conductor is a conductor which is sensitive to the adjacent noisy conductor, wherein the adjacent noisy conductor is capable of being inductively coupled or capacitively coupled to the critical conductor. In order to minimize the coupling between conductor 52 and conductor 54, prior art analyzers route a third conductor 60 from a stable conductor, such as ground conductor 44, to a position adjacent to conductor 52.

Replace the paragraph on page 7, lines 3-8 with the following paragraph:

A method for routing one or more critical conductors in an integrated circuit design is disclosed, including the steps of determining the number of critical [sensitive] conductors requiring placement into preferred [quiet] track locations, wherein a preferred [quiet] track location is defined as any track location immediately adjacent to a constant voltage [stable] conductor, determining the number of preferred [quiet] track locations available in said integrated circuit design, and routing one or more critical [sensitive] conductors into one or more preferred [quiet] track locations.

Replace the paragraph on page 8, lines 6-7 with the following paragraph:

FIG. 6 is a side view of a bit slice of an integrated circuit showing preferred tracks for the placement of critical [sensitive] conductors.

Replace the paragraph on page 8, line 9 with the following paragraph:

FIG. 7 is a flow chart showing the acts performed by the processes of [steps in] a method of the present invention.

Replace the paragraph on page 8, line 18-page 9, line 2 with the following paragraph:

In this disclosure, a constant voltage [stable] conductor shall generally refer to a conductor which does not change state. The examples used in this disclosure of constant voltage [stable] conductors are power and ground. However, those of ordinary skill in the art will readily recognize that other constant voltage [stable] conductors fitting this description exist in the art.

Replace the paragraph on page 9, lines 7-11 with the following paragraph:

Referring to FIG. 5, noisy conductor 54 is placed as previously seen in FIG 3. However, critical conductor 62 is a conductor which is sensitive to inductive or capacitive coupling from an adjacent noisy conductor. [However, conductor 62, a conductor determined to be critically sensitive, has been placed immediately adjacent to stable ground conductor 44.] Noisy conductor 64 although adjacent to conductor 62 does not inductively couple to conductor 62 due to the "quieting" influence on conductor 62 by ground conductor 44.

Replace the paragraph on page 9, lines 13-18 with the following paragraph:

Because integrated circuits are constructed using multiple metal layers, the quieting influence on a critical conductor by a constant voltage [stable] conductor is not restricted to a single metal layer. Therefore, so long as a critical [sensitive] conductor needing a quieting influence [environment] is designed to be placed at a track location immediately adjacent to a constant voltage [stable] conductor, the effects of the quieting influence of the constant voltage [stable] conductor may be felt.

Replace the paragraph on page 10, lines 1-2 with the following paragraph:

FIG. 6 is a side view of a bit slice of an integrated circuit showing preferred tracks for the placement of critical [sensitive] conductors.

Replace the paragraph on page 10, lines 5-9 with the following paragraph:

Referring to FIG. 6, bit slice 70 includes two metal layers 72 and 74, with each of layers 72 and 74 including one or more constant voltage conductors, such as a power conductor 42 and a ground conductor 44. [including a power conductor 42 and a ground conductor 44.] According to one embodiment of the present invention, "quiet" locations for the placement of sensitive conductors include tracks 76a through 76h. These tracks are all immediately adjacent to constant voltage [stable conductors].

Replace the paragraph on page 10, lines 11-17 with the following paragraph:

Tracks such as track 76a, which are immediately adjacent to more than one constant voltage [stable] conductor, are considered to be especially quiet, due to

the increased coupling to more than one constant voltage [stable] conductor. Therefore, tracks 76a, 76c, 76f and 76g are especially quiet, and should be utilized for placement of the most critical [sensitive] conductors, as determined by the IC designer. An IC may have four or more metal layers, providing for potential quiet tracks above, below, left, and right of a given constant voltage [stable] conductor.

Replace the paragraph on page 11, lines 4-11 with the following paragraph:

Referring to FIG. 7, the method begins at block step 80 wherein the signal conductors which need a quieting influence [environment] in which to operate are prioritized. At this step, if a given design is known to have fewer critical [sensitive] lines than preferred tracks to place them, all sensitive conductors may be routed into a preferred location. Alternatively, a designer may rank each critical [sensitive] conductor in order of its importance relative to other sensitive conductors. In this alternative case, conductors are routed according to their rank, thus ensuring that the more highly ranked conductors are placed in quiet track locations.

Replace the paragraph on page 11, lines 13-16 with the following paragraph:

At block [step] 82, it is determined how many preferred tracks exist in the present design. At this step, the analyzer may alternatively rank the preferred tracks, ranking the tracks which are immediately adjacent to two constant voltage [stable] conductors higher than tracks which are immediately adjacent to a single constant voltage [stable] conductor.

Replace the paragraph on page 12, lines 1-9 with the following paragraph:

At block [step] 84, the analyzer routes critical [sensitive] conductors into tracks previously designated at step 82. If, at step 80, the designer had ranked sensitive conductors according to the desirability of placing them in a constant voltage [stable] location, the analyzer routes the higher ranked conductors first. If, at step 82, the analyzer had ranked the preferred tracks according to whether any given preferred track had one, two, or more adjacent constant voltage [stable] conductors, the analyzer, at step 84, places the most highly ranked critical [sensitive] conductor at the most preferred location. The analyzer then places the next highest ranked critical [sensitive] conductor at the next most preferred track location, and so on, until all ranked conductors have been placed.

Replace the paragraph on page 12, lines 11-12 with the following paragraph:

At block [step] 86, the analyzer routes any conductors not already routed into the remaining track locations.

MARKED UP CLAIMS

In the claims kindly amend as follows:

1.(Amended) A method for routing at least one critical conductor [conductors] in an integrated circuit design comprising the steps of:

providing a plurality of logic signals which are communicated by said at least one critical conductor;

determining that at least one conductor is a critical conductor [the number of sensitive conductors] to protect from inductive coupling or capacitive coupling from at least one adjacent conductor [requiring placement into quiet track locations, wherein a quiet track location is defined as any track location immediately adjacent to a stable conductor];

determining the location of at least one preferred track, said preferred track adjacent to a constant voltage conductor [number of quiet track locations available in said integrated circuit design];

routing said at least one critical conductor into said at least one preferred track [one or more sensitive conductors into one or more quiet track locations.]; and

protecting said plurality of logic signals communicated by said at least one conductor from inductive coupling or capacitive coupling by routing said at least one critical conductor.

2.(Amended) The method of claim 1 further comprising the step of:

ranking each of said at least one critical conductor [one or more sensitive conductors] in order of importance relative to other critical conductors [according

to the relative desirability of said one or more sensitive conductors being placed into a quiet environment, as compared to other conductors]; and

wherein said routing step further includes the step of routing said ranked critical conductor [sensitive conductors], according to said ranking.

3.(Amended) The method of claim 2 further comprising the step of:

ranking said at least one [one or more] preferred track location [locations] according to whether said at least one [one or more] preferred track location [locations] are adjacent to at least one [one or more] constant voltage conductor [stable conductors]; and

wherein said routing step further includes the step of routing said ranked at least one critical conductor [sensitive conductors], according to said track location ranking, and said at least one critical [sensitive] conductor ranking.

4.(Amended) A computer system for routing conductors in an integrated circuit design, the computer system comprising:

a processor; and

a memory operatively coupled to said processor having stored therein the following:

means for providing a plurality of logic signals which are communicated by said at least one conductor;

means for determining the number of critical [sensitive] conductors to protect from inductive coupling or capacitive coupling from at least one adjacent conductor [requiring placement into a quiet track location, wherein a quiet track

location is defined as any track location immediately adjacent to a stable conductor];

means for determining the location of at least one preferred track, said preferred track adjacent to a constant voltage conductor [number of quiet track locations available in said integrated circuit design];

means for routing said at least one critical conductor into said at least one preferred track [one or more sensitive conductors into one or more quiet track locations.]; and

means for protecting said plurality of logic signal communicated by said at least one conductor from inductive coupling or capacitive coupling by routing said at least one critical conductor.

5.(Amended) The computer system according to claim 4, the memory further having stored therein the following:

means for ranking each of said at least one critical conductor [one or more sensitive conductors] in order of importance relative to other critical conductors [according to the relative desirability of said one or more sensitive conductors being placed into a quiet environment, as compared to other conductors]; and

means for routing said ranked critical [sensitive] conductors, according to said ranking.

6.(Amended) The computer system according to claim 4, the memory further having stored therein the following:

means for ranking said at least one [one or more] preferred track location [locations] according to whether said at least one [one or more] preferred track locations are adjacent to one or more constant voltage [stable] conductors; and

means for routing said ranked critical [sensitive] conductors, according to said track location ranking, and said critical [sensitive] conductor ranking.

7.(Amended) A machine-readable medium disposed on a computer to perform a method for routing at least one critical conductor [conductors] in an integrated circuit design, the method comprising the steps of:

providing a plurality of logic signals which are communicated by said at least one critical conductor;

determining the number of critical [sensitive] conductors to protect from inductive coupling or capacitive coupling from at least one adjacent conductor [requiring placement into a quiet track location, wherein a quiet track location is defined as any track location immediately adjacent to a stable conductor];

determining the location of at least one preferred track, said preferred track adjacent to a constant voltage conductor [number of quiet track locations available in said integrated circuit design];

routing said at least one critical conductor into said at least one preferred track [one or more sensitive conductors into one or more quiet track locations.]; and

protecting said plurality of logic signals communicated by said at least one conductor from inductive coupling or capacitive coupling by routing said at least one critical conductor.

8.(Amended) The machine-readable medium of claim 7, the method therein further comprising the step of:

ranking each of said at least one critical conductor [one or more sensitive conductors] in order of importance relative to other critical conductors [according to the relative desirability of said one or more sensitive conductors being placed into a quiet environment, as compared to other conductors]; and

wherein said routing step further includes the step of routing said ranked critical [sensitive] conductors, according to said ranking.

9.(Amended) The machine-readable medium of claim 8, the method therein further comprising the step of:

ranking said at least one [one or more] preferred track location [locations] according to whether said at least one [one or more] preferred track location [locations] are adjacent to at least one [one or more] constant voltage conductor [stable conductors]; and

wherein said routing step further includes the step of routing said ranked critical [sensitive] conductors, according to said track location ranking and said critical [sensitive] conductor ranking.